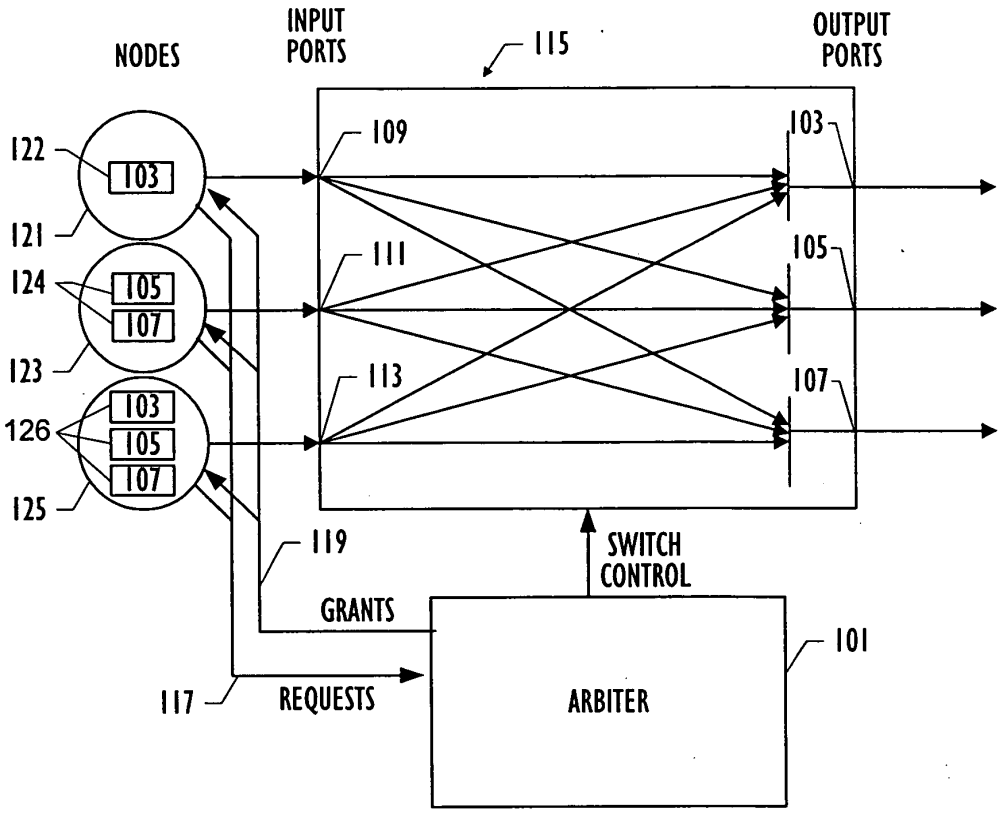

NODES
INPUT PORTS
115
OUTPUT PORTS
122
103
121
124
105
107
123
126
103
105
107
125
109
111
113
103
105
107
119
SWITCH CONTROL
GRANTS
101
117
REQUESTS
ARBITER

FIG. 1

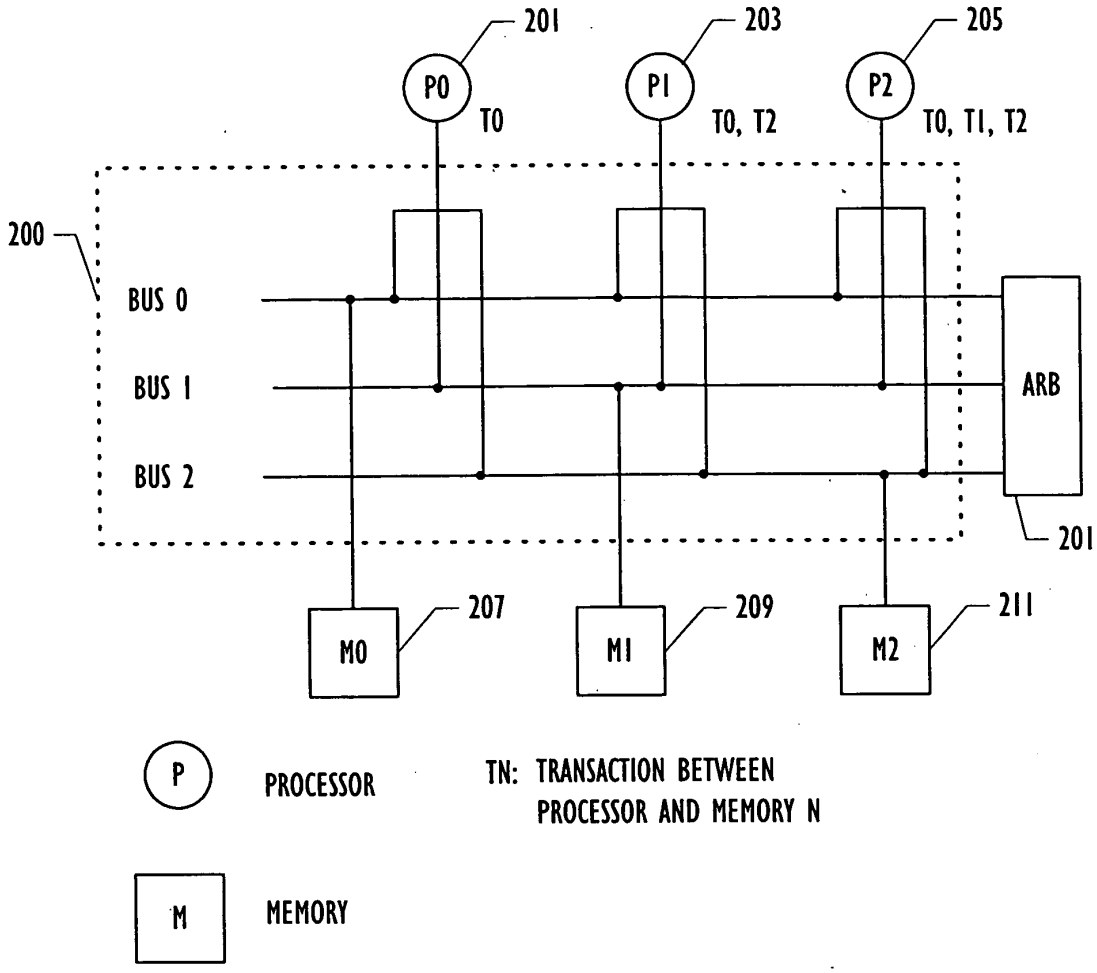
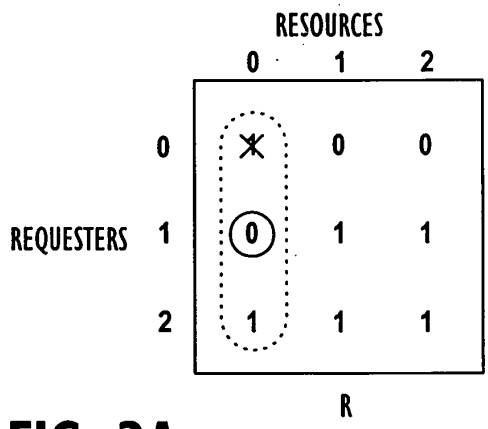

201
203
205
P0
P1
P2
T0
T0, T2
T0, T1, T2
200
BUS 0
BUS 1
BUS 2
ARB
201
207
209
211
M0
M1
M2
P
PROCESSOR
TN: TRANSACTION BETWEEN PROCESSOR AND MEMORY N
M
MEMORY

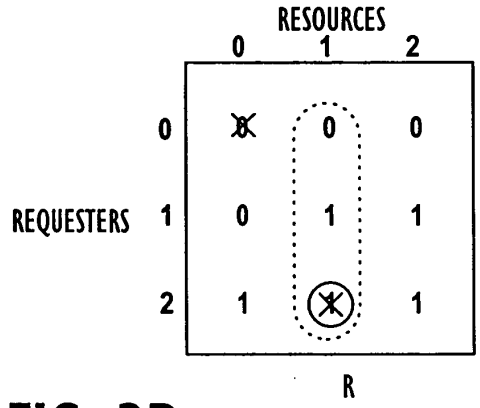
FIG. 2



I	J	RES	NRQ
1	0	0	nrq[0] = 1 nrq[1] = 2 nrq[2] = 3

ROUND-ROBIN POSITION
GRANTED REQUEST

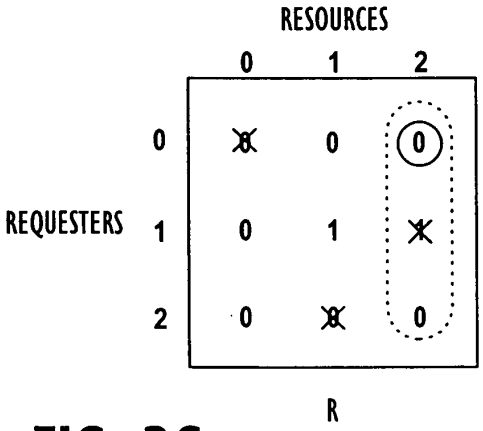
FIG. 3A



I	J	RES	NRQ
1	0	1	nrq[0] = 0 nrq[1] = 2 nrq[2] = 2

ROUND-ROBIN POSITION
GRANTED REQUEST

FIG. 3B



I	J	RES	NRQ
1	0	2	nrq[0] = 0 nrq[1] = 1 nrq[2] = 0

ROUND-ROBIN POSITION
GRANTED REQUEST

FIG. 3C

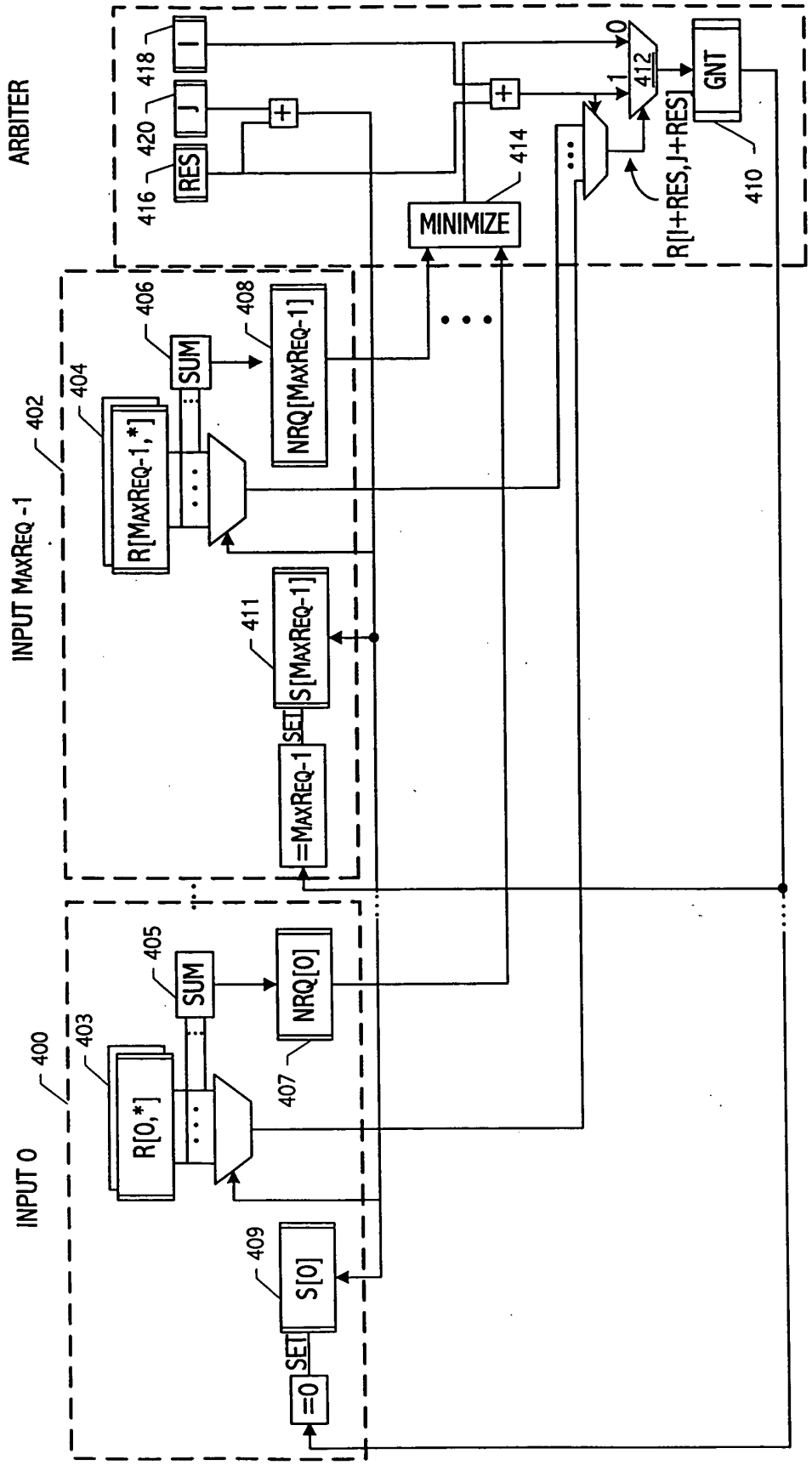
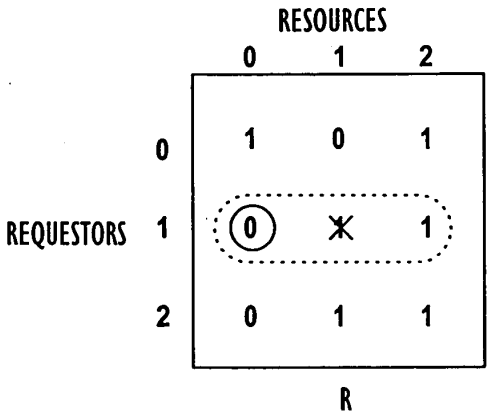

ARBITER
418
I
420
J
416
RES
414
MINIMIZE
412
0
1
GNT
410
R[I+RES,J+RES]
INPUT MAXREQ -1
402
404
R[MAXREQ-1,*]
406
SUM
408
NRQ[MAXREQ-1]
411
S[MAXREQ-1]
SET
=MAXREQ-1
INPUT 0
400
403
R[0,*]
405
SUM
NRQ[0]
407
409
S[0]
SET
=0

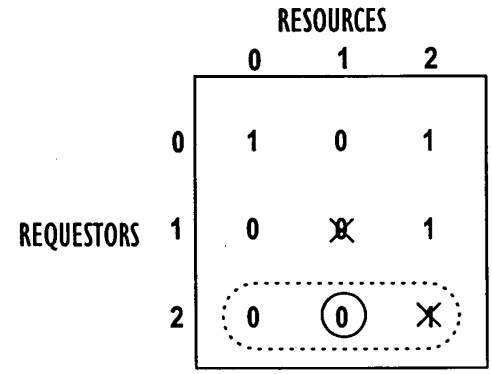
FIG. 4



I	J	REQ	NRQ
1	0	0	nrq[0] = 1 nrq[1] = 2 nrq[2] = 3

○ ROUND-ROBIN POSITION
× GRANTED REQUEST

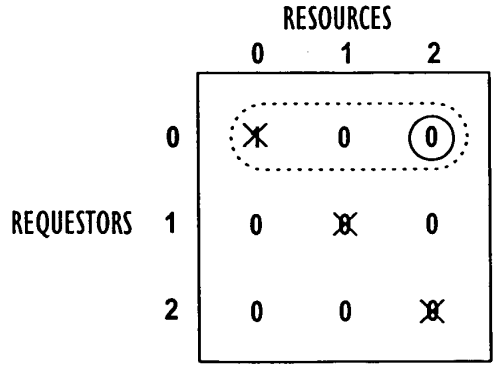
FIG. 5A



I	J	REQ	NRQ
1	0	1	nrq[0] = 1 nrq[1] = 0 nrq[2] = 3

○ ROUND-ROBIN POSITION
× GRANTED REQUEST

FIG. 5B



I	J	REQ	NRQ
1	0	2	nrq[0] = 1 nrq[1] = 0 nrq[2] = 0

○ ROUND-ROBIN POSITION
× GRANTED REQUEST

FIG. 5C

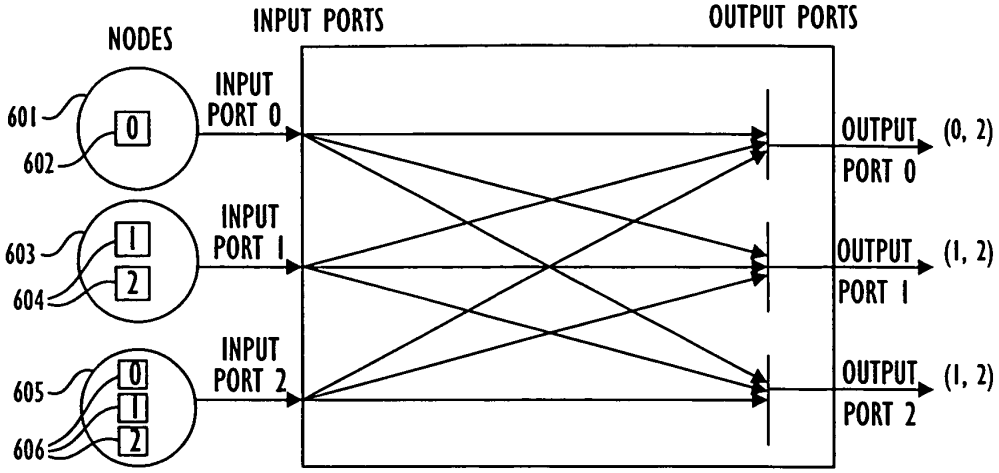


FIG. 6

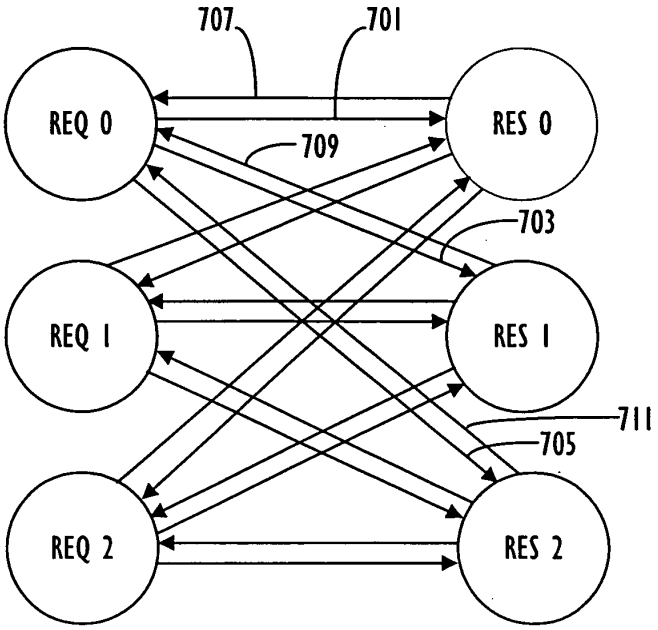


FIG. 7

	Output Port 0	Output Port 1	Output Port 2
REQUEST VECTOR 0	1	0	0
REQUEST VECTOR 1	0	1	1
REQUEST VECTOR 2	1	1	1

FIG. 8